CBCS SCHEME

USN | | | | | | | | | | |

18EC35

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With a neat diagram, explain basic operational concept of computer. **(10 Marks)**

b. Explain in brief different types of key parameters that affect the processor performance. **(05 Marks)**

c. Explain the Bus Structures. **(05 Marks)**

OR

2 a. Illustrate Instruction and Instruction sequencing with an example. **(10 Marks)**

b. Define Byte Addressability, Big-endian and Little-endian assignment. **(06 Marks)**

c. Represent 85.125 in IEEE floating point using single precision. **(04 Marks)**

Module-2

3 a. What is an addressing mode? Explain any five types of addressing modes with example. **(10 Marks)**

b. Write a program to add 'n' number using indirect addressing mode. **(06 Marks)**

c. Explain various assembler directives used in assembly language program. **(04 Marks)**

OR

4 a. Explain stack operation with an example **(10 Marks)**

b. Explain subroutine linkage with an example using linkage register. **(06 Marks)**

c. Explain the shift and rotate operations with example. **(04 Marks)**

Module-3

5 a. Showing the possible register configuration in I/O interface, explain program controlled input/output. **(10 Marks)**

b. What is an interrupt? With an example illustrate the concept of interrupt. **(10 Marks)**

OR

6 a. Explain in detail, the situations where a number of devices capable of initiating interrupts are connected to processor. How to resolve the problems? **(10 Marks)**

b. Explain the registers involved in a DMA interface, to illustrate DMA. **(06 Marks)**

c. Explain the concept of Vectored Interrupt. **(04 Marks)**

Module-4

7 a. With figure, explain Internal Organization of 2M×8 dynamic memory chip. **(10 Marks)**

b. Illustrate Internal structure of static memories. **(10 Marks)**

OR

8 a. With a neat diagram, explain virtual memory organization. **(10 Marks)**

b. Briefly explain any four non-volatile memory concepts. **(05 Marks)**

c. Briefly explain secondary storage devices. **(05 Marks)**

Module-5

9 a. Explain the three-bus organization of the processor and its advantages. **(10 Marks)**

b. Discuss the organization of hardwired control unit. **(05 Marks)**

c. Discuss the control sequence for execution of instruction ADD(R_3), R_1 **(05 Marks)**

OR

10 a. With a block diagram, describe the organization of a micro programmed control unit. **(10 Marks)**

b. Describe the sequence of control signals to be generated to fetch an instruction from memory in a single bus organization. **(10 Marks)**

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